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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/696,117	10/25/2000	Satoshi Kitagawa	83670	4414

7590 06/04/2003

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EXAMINER	
CAPUTO, LISA M	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/696,117	KITAGAWA, SATOSHI	
	Examiner	Art Unit	
	Lisa M Caputo	2876	

-- Th MAILING DATE of this communication appears on th cover she t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 19 May 2003 has been entered.

Amendment

2. Receipt is acknowledged of the amendment filed 19 May 2003.

Claim Objections

3. Claims 1-6 and 8 are objected to because of the following informalities:

Regarding claim 1, line 7: Replace "comprising steps of" with --comprising the step of--.

Regarding claim 2, line 8: Replace "comprising the steps of" with --comprising the step of--.

Regarding claims 1-6 and 8: Replace the word "partially" because partially is a vague, relative term and in this context recited that a mark is "partially effaced" is something that is unable to be easily measured.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "A method of replacing a mark on a semiconductor wafer, the mark replacing an original mark that has been at least partially during...". Examiner understands the concept of the claim and hence the claim is examined because it seems as though through the amendment the word "effaced" between "partially" and "during" was inadvertently crossed out. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 12 and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (U.S. Patent No. 6,312,876, from hereinafter "Huang").

Huang teaches a method for placing identifying marks on semiconductor wafers having all of the elements and means as recited in claims 12 and 24-25 of the instant application.

Regarding claims 12 and 24-25, Huang teaches a method for identifying a wafer during its manufacture, comprising the following steps, etching the wafer a first time in a pattern of small dots that trace a character, the character being human readable but an individual dot being smaller than a human can see, forming a multi-layer structure above the wafer and thereby obscuring the identifying character, and then etching the wafer a subsequent time in the pattern to reestablish the readability of the character (see claim 1). Huang teaches that the letter "T" in this example is a human readable character but from a more general standpoint it is part of the character set that is customarily used for identifying wafers. The letter T is representative of a variety of characters, such as letters and numerals, that are human readable. Other symbols such as a bar code can be formed by the process that will be described later. Ordinarily the wafer identifier will be formed as a block of several characters in order to track a large number of wafers (see Figure 2, col 3 line 8 to col 3 line 17). The bar code consists of two or more similar marks.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11 and 13-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (U.S. Patent No. 6,312,876, from hereinafter "Huang") in view of Yano et al. (U.S. Patent No. 6,268,641, from hereinafter "Yano").

Huang teaches a method for placing an identifying mark on a semiconductor wafer. Huang discloses that the wafer marking tool of this invention uses a fiber optic bundle and an associated optical system to illuminate a photoresist in a pattern for an identifying character. Preferably, a switchable light source is provided for each fiber. These light sources are selectively switched on or off to form a pattern for a character. (In the specific description later, the letter "T" is used as an example.)

A layer of a resist is formed on the wafer and is exposed to the light pattern created by the marking tool. The resist is then developed and the wafer is etched in the pattern of the resist to form an arrangement of small holes that trace the character. The holes are about 100 microns in diameter and about 1 micron deep. The individual dots are too small to be seen, but the character is large enough to be read by operating personnel and by conventional machines for this purpose. The character will ordinarily be etched during an etching step that is performed for wafer manufacture, and etching the character does not interfere with a simultaneous etch that takes place for manufacturing the wafer. The wafer resist is exposed separately for the identifying mark because the mark is unique to a single wafer. During wafer manufacturing, a wafer

etching step is commonly performed several times as a multi-layered structure is formed on the silicon substrate, and the wafer identifier mark becomes obscured by these process steps. Depositing metal on the wafer particularly obscures the mark. The etch step can be repeated without affecting the other steps of the manufacturing process (see col 1 line 46 to col 2 line 10).

FIG. 1 shows part of a wafer 12 that is conventionally circular except for a notch 14 in its edge 13. Notch 14 is a mark for orienting the wafer. Commonly, a wafer identifying character 15 is located near the notch, and the drawing shows the single letter, "T" formed in this region. From a more general standpoint, a set of one or more identifying characters 15 is formed in a suitable region 16 of wafer 12 and this region may be associated with a wafer orienting mark 14. FIG. 2 shows the "T" of FIG. 1 as part of a matrix of circles that represent the light emitting ends of optical fibers. The darkened circles that form the letter "T" represent fibers that are carrying light and the clear circles form the background of the character T and represent the positions of fibers that are not carrying light in this example, as recited in claims 21-22. In this example, the resist is removed where it has been exposed to light carried by the fibers. Similarly, the light sources can be controlled to form the complement of the pattern of FIG. 1 if the resist is removed in the regions that are not exposed to light. Bundle 20 is in the form of an eight by eight orthogonal array of optical fibers. The art of forming characters with such an array is well known from the familiar use of dot arrays for characters on a computer display and in some printers. Any suitable array can be used. As character 15 is represented in FIGS. 1 and 2, the vertical stem and the horizontal

cap of the T are each formed by a double row of dots 18. From a more general standpoint, the outline of the letter is filled with dots. The dots represent circular holes formed in the wafer, but the term "dots" is used here in this description because this terminology will be familiar from other dot matrix characters such as a computer display and a dot matrix printer. The letter "T" in this example is a human readable character but from a more general standpoint it is part of the character set that is customarily used for identifying wafers. The letter T is representative of a variety of characters, such as letters and numerals, that are human readable. Other symbols such as a bar code can be formed by the process that will be described later. Ordinarily the wafer identifier will be formed as a block of several characters in order to track a large number of wafers (see Figure 2, col 2, lines 47 to col 3 line 17). The dots 18 are larger than many features created using photoresist, and they can be formed as part of a conventional etch process that is performed primarily for producing devices on the wafer and only secondarily used for producing the wafer identifying characters. Ordinarily, other regions of the resist, not represented in the drawing, will be exposed according to a desired pattern that is independent of dots 18. Exposed regions 42, 43 of the photoresist layer 36 are removed when the photoresist is developed, and remaining regions 44 of layer 36 mask the underlying regions of the wafer. The wafer surface is etched in any suitable way, as established for the accompanying step of the wafer manufacturing process. FIG. 5 shows the wafer 12 of FIG. 4 after the etch step. Holes 45 and 46 form two of the dots of the characters illustrated in FIGS. 1, 2 and 3. A dot 45, 46 is about 100 microns in diameter and about 1 micron deep. Thus, a dot is too small to be resolved by the

human eye. A character (15 in FIG. 1) is preferably of a size to be human readable and the characters are readable by machines constructed for this purpose. A typical wafer mark has about 13 characters and is about 13 millimeters in length. The tool of FIG. 4 exposes the resist for a single character at a time, but it illustrates all of the features of a tool for producing the entire character block with one exposure (see Figure 4B, col 4 lines 36-64).

In essence, Huang teaches a method for identifying a wafer during its manufacture, comprising the following steps, etching the wafer a first time in a pattern of small dots that trace a character, the character being human readable but an individual dot being smaller than a human can see, forming a multi-layer structure above the wafer and thereby obscuring the identifying character, and then etching the wafer a subsequent time in the pattern to reestablish the readability of the character (see claim 1).

Regarding claims 1-4, Huang fails to teach that the new mark is formed at another location spaced apart from the partially-effaced mark with the purpose of replacing the original mark.

Yano teaches a semiconductor wafer having identification indication and method of manufacturing the same. Yano discloses that FIG. 18 is a plan view of the semiconductor wafer surface with the engraving formed thereon. FIG. 19 is an enlarged cross-sectional view of a part of the engraved portion. If the engraving is formed on the surface of the semiconductor wafer 104 by the laser beam radiation, actually not only the groove but also a bump (uplift) 202 is formed in the engraved portion as shown in

FIG. 19. Due to the bump 202, the homogeneity of the flatness is deteriorated in the subsequent CMP treatment. That is, since an abrading pad (not illustrated) of an abrading device cannot or hardly makes contact with the rear part of the semiconductor wafer 104 at the time of contacting and abrading the bump 202 of the engraved portion due to the height of the bump 202, an under polish is generated on the semiconductor wafer surface portion in the vicinity of the bump 202. Furthermore, when attaching such a wafer with a bump on a stage in a stepper, the bump portion of the wafer rises so that the light beam cannot be focused well in the lithography. FIG. 20 is a side view of the semiconductor wafer 104 where the identification indication 16 is formed by engraving the rear surface of the semiconductor wafer 104 by the laser beam radiation. The rear surface of the semiconductor is, however, applied with the wrapping treatment (backside grinding) preceding the packaging, and thus by the wrapping treatment, the wafer 104 (such as a silicon substrate) usually having about 725 um thickness becomes thinner to about 300 um thickness. By the wrapping treatment, the identification indication 16 by engraving is completely eliminated without remaining until the cutting and separating process of the wafer 104 into chips.

As heretofore mentioned, in the case the identification indication 16 is formed on the surface of the wafer, the outline of the engraving on the semiconductor wafer surface disappears or becomes unclear by the subsequent processes on the wafer surface for forming a semiconductor circuit so that it becomes difficult to read the identification indication 16. On the other hand, in the case the identification indication 16 is formed on the rear side of the wafer, the identification indication 16 by engraving

completely disappears by the wrapping treatment of the wafer rear surface preceding the packaging and thus it is impossible to read the identification indication 16 (see Figures 18-20, col 2, lines 10-51). In order to solve the above-mentioned problems, an object of the present invention is to provide a semiconductor wafer having an identification indication capable of maintaining the identification indication formed by engraving in a clearly recognizable state until the wafer is cut and separated into chips without having the identification indication for identifying the wafer disappear or become unclear even after the treatment process on the wafer surface for forming a semiconductor circuit, or even after the treatment process after the wrapping treatment process on the wafer rear surface, and a method of manufacturing a semiconductor wafer having an identification indication. In order to achieve the above-mentioned object, in the present invention, the identification indication for identifying the semiconductor wafer is formed on a selected side surface portion of the semiconductor wafer to remain after performing the semiconductor wafer abrading treatment from the rear side for making the semiconductor wafer thinner.

The present invention is to provide a semiconductor wafer having a semiconductor wafer identification indication on a selected side surface portion of the semiconductor wafer to remain after performing the semiconductor wafer abrading treatment from the rear side for making the semiconductor wafer thinner. The side surface of the semiconductor wafer may have a slant face portion elongating from the front surface, a slant face portion elongating from the rear surface, and a peripheral surface portion between the slant face portion elongating from the front surface and the

slant face portion elongating from the rear surface, and the selected side surface portion may be the slant face portion elongating from the front surface. The side surface of the semiconductor wafer may have a slant face portion elongating from the front surface, a slant face portion elongating from the rear surface, and a peripheral surface portion between the slant face portion elongating from the front surface and the slant face portion elongating from the rear surface, and the selected side surface portion may be a portion at the side close to the slant face portion elongating from the front surface. The identification indication may be an engraving formed on the selected side surface portion of the semiconductor wafer. The engraving may be formed by the laser beam radiation to the selected side surface portion of the semiconductor wafer. The identification indication may include an indication readily recognized visibly. The identification indication readily recognized visibly may include a numeral, a mark, and the like. The identification indication may include an indication readily recognized optically. The identification indication may include an identification indication readily recognized by a laser beam. The indication readily recognized optically or by a laser beam may include a bar code...Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims (see col 2 line 54 to col 4 line 19).

FIGS. 1 and 2 show a side surface 14 of a wafer 12 of a first embodiment of the present invention. FIGS. 1 and 2 show an indication 16 (identification indication) for identifying the wafer 12 formed on a selected portion (selected side surface portion) 18 of the wafer side surface 14 in the front and the side, respectively. The wafer 12 is applied with an independent identification indication 16 for identifying the semiconductor wafer 12 before the semiconductor circuit forming treatment. The identification indication 16 is formed by engraving the semiconductor wafer 12 by the laser beam radiation so as to be recognized by the outline of the engraving. The identification indication 16 includes a combination of bar codes appropriate for reading optically and numerals and alphabets appropriate for reading visibly. Unlike conventional technology, the indication is not formed on the front surface or the rear surface of the semiconductor wafer 12 as in the first embodiment, but on the selected side surface portion 18 of the semiconductor wafer 12 by engraving by the laser beam radiation in this invention as shown in FIGS. 1 and 2. Various treatment processes are conducted for forming the semiconductor circuit in each chip area on the surface of the semiconductor wafer 12 with the identification indication 16 formed thereon. The treatment processes include abrading or flattening processes such as an oxide film formation process, a metal film formation process, a heating process, a resist application process, a piercing process, a lithography process, an ion injection process, a CMP, and the like. In the case the identification indication 16 defined by the engraving outline is formed on the surface of the semiconductor wafer 12 in the conventional technology, the outline of the identification indication 16, that is, the engraving disappears or becomes unclear by the

treatment processes so that it cannot be recognized. Moreover, a wrapping treatment is applied on the semiconductor wafer 12 from the rear surface preceding the packaging. By the wrapping treatment, the wafer 12 is thinned from, in general, about 725 um to about 300 um. That is, the wafer 12 becomes thinner. By the wrapping treatment, in the case the identification indication 16 is formed on the rear surface of the semiconductor wafer 12 as in the conventional technology, the identification indication 16 completely disappears. However, unlike the conventional technology, since the identification indication 16 is not formed on the front surface or the rear surface of the semiconductor wafer 12, but on the side surface 14 of the semiconductor wafer 12 as shown in FIGS. 1 and 2 (the first embodiment) in the present invention. More specifically, the identification indication 16 is formed on the selected side surface portion 18 of the semiconductor wafer 12. Since the identification indication 16 is formed on the side surface 14 of the semiconductor wafer 12, even if various treatment processes are repeatedly conducted for forming a semiconductor circuit in each chip area on the wafer 12 surface as in the conventional technology, the identification indication 16, that is, the engraving cannot disappear or become unclear by the treatment processes. Moreover, the engraving formed on the selected side surface portion 18 of the side surface 14 of the semiconductor wafer 12 cannot disappear or become unclear by the wrapping treatment on the rear surface of the semiconductor wafer 12. Accordingly, since the identification indication 16 is formed on the side surface 14 of the semiconductor wafer 12 as shown in FIGS. 1 and 2 but not on the front surface or the rear surface of the semiconductor wafer 12, the identification indication 16 formed on the side surface 14 of the

semiconductor wafer 12 cannot disappear or become unclear but can be maintained so as to be recognizable clearly even if various treatment processes are repeatedly conducted for forming a semiconductor circuit in each chip area on the wafer 12 surface as in the conventional technology, or by the wrapping treatment on the rear surface of the semiconductor wafer 12. Accordingly, the identification indication 16 by engraving can be maintained to be recognized sufficiently clearly until the process where the wafer 12 is cut into chips. The identification indication 16 is preferably engraved by a laser beam radiation as in the conventional technology (see Figures 1-2, col 5 line 62 to col 7 line 4). In essence, Yano teaches a method to be able to identify a wafer through manufacturing processes.

In view of the teaching of Yano, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the mark at a spaced apart location to ensure that at least one of the marks was still available to read to replace the original mark should it be partially-effaced. This is favorable because then the wafer could be able to be checked via two means of identification. In addition, the entire wafer would be utilized for identification purposes so that if an anomaly should occur and one of the identification markings does become unattainable, there are identification marks on different parts of the body of the semiconductor wafer, increasing the chances for a readable mark.

Regarding claims 5-6, 10-11, and 17-22, Huang teaches that a layer of a resist is formed on the wafer and is exposed to the light pattern created by the marking tool. The resist is then developed and the wafer is etched in the pattern of the resist to form an

arrangement of small holes that trace the character. The holes are about 100 microns in diameter and about 1 micron deep. The individual dots are too small to be seen, but the character is large enough to be read by operating personnel and by conventional machines for this purpose (see col 1, lines 53-62). Huang teaches holes about 100 microns in diameter and about 1 micron deep, which is along the same order as 1 to 13 micrometers.

Regarding claims 7-11, Huang fails to specifically teach that the notch has identification marks reproduced on it.

Huang discloses that FIG. 1 shows part of a wafer 12 that is conventionally circular except for a notch 14 in its edge 13. Notch 14 is a mark for orienting the wafer. Commonly, a wafer identifying character 15 is located near the notch, and the drawing shows the single letter, "T" formed in this region. From a more general standpoint, a set of one or more identifying characters 15 is formed in a suitable region 16 of wafer 12 and this region may be associated with a wafer orienting mark 14 (see Figure 1, col 2, lines 34-43).

In view of the teaching of Huang and with ordinary skill in the art, it would have been obvious to one of ordinary skill in the art at the time the invention was made to affix a mark in the interior wall surface of the notch because the notch is a somewhat protected area of the semiconductor wafer and hence the mark would be protected as well. It is favorable to have multiple marks at different places on the wafer so that the chance for having a readable mark after processing is increased.

Regarding claim 13, Huang teaches that during wafer manufacturing, a wafer etching step is commonly performed several times as a multi-layered structure is formed on the silicon substrate, and the wafer identifier mark becomes obscured by these process steps. Depositing metal on the wafer particularly obscures the mark. The etch step can be repeated without affecting the other steps of the manufacturing process (see col 2 line 4 to col 2 line 10). During the wafer manufacturing the different steps comprise different speeds.

Regarding claims 14-18 and 20-23, Huang teaches that the letter "T" in this example is a human readable character but from a more general standpoint it is part of the character set that is customarily used for identifying wafers. The letter T is representative of a variety of characters, such as letters and numerals, that are human readable. Other symbols such as a bar code can be formed by the process that will be described later. Ordinarily the wafer identifier will be formed as a block of several characters in order to track a large number of wafers (see Figure 2, col 3 line 8 to col 3 line 17). The bar code will inevitably consist of two or more similar marks (in a single direction as recited in claim 23) and is readable by a single optical reading machine. In addition, Huang teaches that during wafer manufacturing, a wafer etching step is commonly performed several times as a multi-layered structure is formed on the silicon substrate, and the wafer identifier mark becomes obscured by these process steps. Depositing metal on the wafer particularly obscures the mark. The etch step can be repeated without affecting the other steps of the manufacturing process (see col 2 line 4

to col 2 line 10). During the wafer manufacturing the different steps comprise different speeds.

Regarding claims 14-18 and 20-23, Huang fails to teach that marks are provided on the front and reverse sides of the wafer.

Yano teaches a semiconductor wafer having identification indication and method of manufacturing the same. Yano discloses a conventional process where that FIG. 18 is a plan view of the semiconductor wafer surface with the engraving formed thereon. FIG. 19 is an enlarged cross-sectional view of a part of the engraved portion. If the engraving is formed on the surface of the semiconductor wafer 104 by the laser beam radiation, actually not only the groove but also a bump (uplift) 202 is formed in the engraved portion as shown in FIG. 19. Due to the bump 202, the homogeneity of the flatness is deteriorated in the subsequent CMP treatment. That is, since an abrading pad (not illustrated) of an abrading device cannot or hardly makes contact with the rear part of the semiconductor wafer 104 at the time of contacting and abrading the bump 202 of the engraved portion due to the height of the bump 202, an under polish is generated on the semiconductor wafer surface portion in the vicinity of the bump 202. Furthermore, when attaching such a wafer with a bump on a stage in a stepper, the bump portion of the wafer rises so that the light beam cannot be focused well in the lithography. FIG. 20 is a side view of the semiconductor wafer 104 where the identification indication 16 is formed by engraving the rear surface of the semiconductor wafer 104 by the laser beam radiation. The rear surface of the semiconductor is, however, applied with the wrapping treatment (backside grinding) preceding the

packaging, and thus by the wrapping treatment, the wafer 104 (such as a silicon substrate) usually having about 725 um thickness becomes thinner to about 300 um thickness. By the wrapping treatment, the identification indication 16 by engraving is completely eliminated without remaining until the cutting and separating process of the wafer 104 into chips (see Figures 18-20, col 2 lines 10-39).

In view of the teaching of Yano, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the marks on different sides of the wafer to ensure that at least one of the marks was still available to read (and not in the part that was effaced). This is favorable because then the wafer could be able to be checked via two means of identification. In addition, the entire wafer would be utilized for identification purposes so that if an anomaly should occur and one of the identification markings does become unattainable, there are identification marks on different parts of the body of the semiconductor wafer, increasing the chances for a readable mark.

Regarding claim 19, Huang discloses that FIG. 1 shows part of a wafer 12 that is conventionally circular except for a notch 14 in its edge 13. Notch 14 is a mark for orienting the wafer. Commonly, a wafer identifying character 15 is located near the notch, and the drawing shows the single letter, "T" formed in this region. From a more general standpoint, a set of one or more identifying characters 15 is formed in a suitable region 16 of wafer 12 and this region may be associated with a wafer orienting mark 14 (see Figure 1, col 2, lines 34-43). Huang teaches that the letter "T" in this example is a human readable character but from a more general standpoint it is part of the character

set that is customarily used for identifying wafers. The letter T is representative of a variety of characters, such as letters and numerals, that are human readable. Other symbols such as a bar code can be formed by the process that will be described later. Ordinarily the wafer identifier will be formed as a block of several characters in order to track a large number of wafers (see Figure 2, col 3 line 8 to col 3 line 17). The bar code will inevitably consist of two or more similar marks and will be readable by a single optical scanner. Huang teaches that during wafer manufacturing, a wafer etching step is commonly performed several times as a multi-layered structure is formed on the silicon substrate, and the wafer identifier mark becomes obscured by these process steps. Depositing metal on the wafer particularly obscures the mark. The etch step can be repeated without affecting the other steps of the manufacturing process (see col 2 line 4 to col 2 line 10). During the wafer manufacturing the different steps comprise different speeds.

Regarding claim 19, Huang fails to teach that the notch has identification marks reproduced on it and that marks are provided on the front side of the wafer.

Yano teaches a semiconductor wafer having identification indication and method of manufacturing the same. Yano discloses a conventional process where that FIG. 18 is a plan view of the semiconductor wafer surface with the engraving formed thereon. FIG. 19 is an enlarged cross-sectional view of a part of the engraved portion. If the engraving is formed on the surface of the semiconductor wafer 104 by the laser beam radiation, actually not only the groove but also a bump (uplift) 202 is formed in the engraved portion as shown in FIG. 19. Due to the bump 202, the homogeneity of the

flatness is deteriorated in the subsequent CMP treatment. That is, since an abrading pad (not illustrated) of an abrading device cannot or hardly makes contact with the rear part of the semiconductor wafer 104 at the time of contacting and abrading the bump 202 of the engraved portion due to the height of the bump 202, an under polish is generated on the semiconductor wafer surface portion in the vicinity of the bump 202. Furthermore, when attaching such a wafer with a bump on a stage in a stepper, the bump portion of the wafer rises so that the light beam cannot be focused well in the lithography. FIG. 20 is a side view of the semiconductor wafer 104 where the identification indication 16 is formed by engraving the rear surface of the semiconductor wafer 104 by the laser beam radiation. The rear surface of the semiconductor is, however, applied with the wrapping treatment (backside grinding) preceding the packaging, and thus by the wrapping treatment, the wafer 104 (such as a silicon substrate) usually having about 725 um thickness becomes thinner to about 300 um thickness. By the wrapping treatment, the identification indication 16 by engraving is completely eliminated without remaining until the cutting and separating process of the wafer 104 into chips (see Figures 18-20, col 2 lines 10-39).

In view of the teaching of Huang and with ordinary skill in the art, it would have been obvious to one of ordinary skill in the art at the time the invention was made to affix a mark in the interior wall surface of the notch because the notch is a somewhat protected area of the semiconductor wafer and hence the mark would be protected as well. It is favorable to have multiple marks at different places on the wafer so that the chance for having a readable mark after processing is increased.

In addition, in view of the teaching of Yano, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the marks on different sides of the wafer to ensure that at least one of the marks was still available to read (and not in the part that was effaced). This is favorable because then the wafer could be able to be checked via two means of identification. In addition, the entire wafer would be utilized for identification purposes so that if an anomaly should occur and one of the identification markings does become unattainable, there are identification marks on different parts of the body of the semiconductor wafer, increasing the chances for a readable mark.

Response to Arguments

7. Applicant's arguments filed 19 May 2003 have been fully considered.

Examiner acknowledges the comments and appreciates the clarification of how the second mark replaces the first mark, however, these limitations appear in the preamble only and should be elaborated upon within the body of the claim along with the other limitations.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***Lisa M. Caputo*** whose telephone number is **(703) 308-8505**. The examiner can normally be reached between the hours of 8:30AM to 5:00PM Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 703-305-3503. The fax phone number for this Group is (703)308-7722, (703)308-7724, or (703)308-7382.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**lisa.caputo@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

LMC
May 30, 2003

THIEN M. LE
PRIMARY EXAMINER